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Thesis Title: - Spintronics-Based Neuromorphic Computing: New Devices and Architectures

Abstract: -

This thesis presents the study, design, and implementation of neural networks using spintronic devices. The first part of this thesis focuses on the spiking neural network, a novel neural-network architecture which is inspired by brain. Spiking Neural Network (SNN) has been shown to consume very low power for an inference task, i.e., forward computation on the test data with a pre-trained model. However, training of such SNN has remained a challenge. In this thesis, Spike-Time-Dependent Plasticity-based (STDP) learning has been used to train the SNN through implementation on an analog hardware using spintronic devices (on-chip learning).

Here, I design and simulate the synapses and neurons in the analog hardware using a combination of ferromagnetic-metal-heavy-metal-based spintronic devices and transistor-based electronic circuits. The spintronic devices have been modeled through micromagnetics and the circuits through SPICE, with the spintronic-device models incorporated inside SPICE as Verilog A modules. Two different modes have been used for the training/ learning: completely unsupervised learning and partially supervised learning (both STDP-enabled but with different level of control over spiking of the output-stage neurons or post-neurons). High classification accuracy is obtained on the popular Fisher's Iris data set of flowers, for both modes of learning.

Next, the SNN is trained on the MNIST data set of handwritten digits. The architecture used by me has less number of network layers that that used previously for MNIST classification. Finally, the time and total energy consumed in the designed synapse circuits,to enable the learning, have been reported.

In the later part of the thesis, a ferrimagnetic domain-wall synapse device has been proposed as an alternative to a ferromagnetic domain-wall synapse device for faster and more energy-efficient on-chip learning on a crossbar-array-based analog-hardware neural network, which uses such synapse devices. Using micromagnetics, domain-wall motion has been modeled for a Co-Gd-bilayer-based device, in which ferrimagnetic-domain-wall motion has been reported experimentally earlier. Then, this domain-wall-based spintronic device model has been incorporated, as a Verilog A module, in the SPICE design of a crossbar-array-based fully connected neural network (FCNN), for each synapse in the crossbar array. It is shown that for the same duration of current pulses needed to move the domain wall and update the synaptic weight for on-chip learning, total energy consumption in the synapses for on-chip learning is five times (5X) lower in the ferrimagnetic-synapse-based FCNN compared to the ferromagnetic-synapse-based FCNN. Similarly, for the same amount of energy consumed for learning, time taken for on-chip learning is five times (5X) lower for the the ferrimagnetic-synapse-based FCNN compared to the ferromagnetic-synapse-based FCNN. Both these results are a consequence of faster domain-wall motion in the ferrimagnetic device compared to the ferromagnetic device.